



Differences Between Hi3521 and Hi3531 SDKs

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About This Document

Purpose

This document describes the differences between Hi3521 and Hi3531 SDKs from the aspects of specifications, software development kit (SDK) components, and application programming interfaces (APIs).

Related Versions

The following table lists the product versions related to this document.

| Product Name | Version |
|--------------|---------|
| Hi3521 | V100 |
| Hi3531 | V100 |

Change History

Updates between document issues are cumulative. Therefore, the latest document issue contains all updates made in previous issues.

Issue 01(2012-08-30)

This issue is the fourth draft release, which incorporates the following changes:

Chapter 1 SDK Differences

The descriptions are updated.

In Table 1-1, the video decoding protocols for the Hi3521 and Hi3531 are updated.

Issue 00B03(2012-04-20)

This issue is the third draft release, which incorporates the following changes:

Chapter 1 SDK Differences

The descriptions are updated.



Issue 00B02 (2012-03-29)

This issue is the second draft release, which incorporates the following changes:

Chapter 1 SDK Differences

The descriptions are updated.

Issue 00B01 (2012-03-20)

This issue is used for first draft release.



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1 SDK Differences

The Hi3521 is a professional high-end system-on-chip (SoC) designed for multi-channel D1 and high-definition (HD) digital video records (DVRs) and network video recorders (NVRs). The Hi3521 SDK is optimized based on the Hi3531 SDK for specific application scenarios. This chapter describes the differences between the Hi3521 and the Hi3531 and the changes of SDK components and APIs for media processing.

1.1 Differences on Specifications

[Table 1-1](#) describes the specifications differences between the Hi3521 and the Hi3531/Hi3532. For details, see the *Hi3521 H.264 Codec Processor Data Sheet*.

Table 1-1 Differences on specifications

| Specifications | Hi3521 | Hi3531/Hi3532 |
|----------------|--|--------------------------------------|
| Processor | ARM Cortex A9 single core@Max. 930 MHz | ARM Cortex A9 dual cores@Max 930 MHz |



| Specifications | Hi3521 | Hi3531/Hi3532 |
|-------------------|--|--|
| Video input (VI) | <ul style="list-style-type: none">• Four VI devices• 16 primary VI channels, no secondary channels. The output resolution of each primary channel can be dynamically changed. The pictures with two resolutions can be captured at the same time.• At most 10D1+6x2CIF real-time inputs.• The supported timings include:<ul style="list-style-type: none">a) 4xBT.656@108 MHz/144 MHz for 16CIF/8x960H real-time video inputsb) 2xBT.1120@148.5 MHz for 2-channel 1080p@30 fps or 2-channel 720p@30 fps/60 fps video inputsc) 4xmultiplexed BT.656@148.5 MHz for 4-channel 720p@30 fps video inputs | <ul style="list-style-type: none">• Eight VI devices• 16 primary VI channel. The channels with even channel IDs have corresponding secondary channels. The output resolution of each primary VI channel or secondary VI channel can be dynamically changed. The pictures with two resolutions cannot be captured at the same time.• Supported timings include:<ul style="list-style-type: none">a) 4xBT.656@108 MHz/144 MHz or 8xBT.656@54 MHz/72 MHz for 16D1/960H real-time video inputsb) 8xBT.656@27 MHz/36 MHz for 8D1/960H real-time video inputsc) 4xBT.1120@148.5 MHz for 4-channel 1080p@30 fps or 4-channel 720p@30 fps/60 fps video inputsd) 8xmultiplexed BT.656@148.5 MHz for 8-channel 720p@30 fps video inputs |
| Video output (VO) | <ul style="list-style-type: none">• Three VO devices, including one HD device and two standard-definition (SD) devices• VGA, HDMI, and LCD (or BT.1120) outputs share the same source. At most 1080p@60 fps• Composite video broadcast signal (CVBS) and BT.656 outputs share the same source. (When LCD is used, BT.656 is not supported.)• One hardware cursor layer in RGB1555 or RGB8888 format, with the maximum resolution of 128x128 | <ul style="list-style-type: none">• Eight VO devices, including two HD devices and six SD devices• HDMI 1.3+VGA/YPbPr +CVBSx2 video outputs. The HDMI and VGA outputs can share the same source.• 8xBT.656@27 MHz output interface• 1080p@ 60 fps for HDMI output• 2560x1600@60 fps for VGA output• Two hardware cursor layers in RGB1555 or RGB8888 format, with the maximum resolution of 128x128 |



| Specifications | Hi3521 | Hi3531/Hi3532 |
|----------------------------|---|---|
| Video pre-processing (VPP) | <ul style="list-style-type: none">• De-interlace, image enhancement, 3D denoising (separate spatial domain denoising for encoding and previewing), sharpening• Eight on-screen displays (OSDs) for each encoding channel, supporting automatic color inverse | <ul style="list-style-type: none">• De-interlace, image enhancement, edge enhancement, and three-dimensional (3D) denoising• Eight OSDs for each encoding channel, supporting automatic color inverse |
| Video encoding protocol | <ul style="list-style-type: none">• H.264 Baseline Profile Level 5.0• H.264 Main Profile Level 5.0• JPEG Baseline | <ul style="list-style-type: none">• H.264 Baseline Profile Level 5.0• H.264 Main Profile Level 5.0• H.264 High Profile Level 5.0• JPEG Baseline |
| Video decoding protocol | <ul style="list-style-type: none">• H.264 Baseline Profile Level 5.0• H.264 Main Profile Level 5.0• H.264 High profile Level 5.0• MPEG4 SP L0~L3• MPEG4 ASP L0~L5/MPEG4 short header• MJPEG/JPEG Baseline | <ul style="list-style-type: none">• H.264 Baseline Profile Level 5.0• H.264 Main Profile Level 5.0• H.264 High Profile Level 5.0• MPEG4 SP L0~3• MPEG4 ASP L0~5/MPEG4 short header• MPEG2 MP/HL, ML, LL• MPEG2 SP/ML• MPEG1• AVS Jizhun Level 6.0• MJPEG/JPEG Baseline |



| Specifications | Hi3521 | Hi3531/Hi3532 |
|--------------------------------|--|--|
| Video encoding and decoding | <p>The NTSC norm is considered when the SD resolution is involved.</p> <ul style="list-style-type: none">• 16CIF@30 fps+16QCIF@30 fps encoding+16CIF@30 fps decoding+JPEG snapshot D1@8 fps• 1x720p@30 fps+VGA@30 fps encoding+7D1@30 fps+ 7CIF@30 fps encoding+1D1@30 fps decoding+JPEG snapshot@4 fps• 8x960H@30 fps+8CIF@30 fps encoding+1x960H@30 fps decoding+JPEG snapshot 960H@4 fps• 8D1@30 fps+8CIF@30 fps encoding+4D1@30 fps decoding+JPEG snapshot D1@4 fps• 1x720p@30 fps+VGA@30 fps encoding+4D1@30 fps+ 4CIF@30 fps encoding+4D1@30 fps decoding+JPEG snapshot@4 fps• 4x960H@30 fps+4CIF@30 fps encoding+4x960H@30 fps decoding+JPEG snapshot 960H@4 fps | <p>The NTSC norm is considered when the SD resolution is involved.</p> <ul style="list-style-type: none">• 16D1@30 fps+16CIF@30 fps encoding+4D1@30 fps decoding+JPEG snapshot D1@16 fps• 4x1080p@30 fps+4x(960x540)@15 fps encoding+1x1080p@30 fps decoding+JPEG snapshot 1080p@4 fps• 4x1080p@15 fps+4x(960x540)@15 fps encoding+4x1080p@15 fps decoding+JPEG snapshot 1080p@4 fps• 4x720p@30 fps+4xQVGA@30 fps encoding+4x720p@30 fps decoding+JPEG snapshot 720p@4 fps• 8x720p@15 fps+8xQVGA@15 fps encoding+8x720p@15 fps decoding+JPEG snapshot 720p@8 fps• 16D1@30 fps decoding• 16x960H@30 fps decoding• 8x720p@30 fps decoding• 4x1080p@30 fps decoding |
| Audio | <ul style="list-style-type: none">• Four standard inter-IC sound (I²S) interfaces. Two interfaces support only input, one interface supports I/O, and the other one supports HDMI I²S output.• ADPCM, G.711, or G.726 encoding is supported. | <ul style="list-style-type: none">• Five standard I²S interfaces. Three interfaces support only input, one interface supports I/O, and the other one supports HDMI I²S output.• ADPCM, G.711, or G.726 encoding is supported. |
| Motion detection | <ul style="list-style-type: none">• Sum of absolute difference (SAD) and motion vector (MV)• Occlusion detection | Sum of absolute difference (SAD) and motion vector (MV) |
| Intelligent video engine (IVE) | The same as the Hi3531 | Integrated IVE, providing motion detection, boundary guard, face detection, and video diagnosis |



| Specifications | Hi3521 | Hi3531/Hi3532 |
|--|---|--|
| Double-data rate (DDR) interface | One 16- or 32-bit DDR2/DDR3 synchronous dynamic random access memory (SDRAM) interface 1 GB maximum capacity | Two 32-bit DDR2 or DDR3 SDRAM interfaces 1 GB maximum capacity for each interface |
| Flash memory | The same as the Hi3531 | SPI NOR flash and NAND flash |
| Network | One gigabit media access controller (GMAC) interface, supporting TCP/IP offload engine (TOE) acceleration | Two GMAC interfaces, supporting TOE acceleration |
| Peripheral component interconnect express (PCIe) | No PCIe interface | Two PCIe 1.1 interfaces |
| Serial advanced technology attachment (SATA) | The same as the Hi3531 | Two SATA 2.6 interfaces |
| Boot modes | No PCIe boot mode | BOOTROM boot mode SPI NOR flash boot mode PCIe boot mode NAND flash boot mode |

1.2 Differences on SDK Components

Table 1-2 describes the differences on SDK components.

Table 1-2 Differences on SDK components

| Component | Hi3521 | Hi3531/Hi3532 |
|-----------|------------------------|--|
| GCC | The same as the Hi3531 | GCC-4.4. It supports embedded application binary interface (EABI), which differs from the old application binary interface (OABI) for GCC-3.3 in aspects of structure byte alignment, function calling mode, and system calling mode. The EABI has better performance and compatibility than the OABI. The latest Glibc does not support the OABI. |



| Component | Hi3521 | Hi3531/Hi3532 |
|---------------------------------|---|--|
| Linux | Linux-3.0.y, supporting Cortex A9 single core | Linux-3.0.y SMP, supporting Cortex A9 dual cores |
| Driver | No difference from the user perspective | None |
| Media processing platform (MPP) | For details, see section 1.3 "Differences on APIs." | None |

1.3 Differences on APIs

Table 1-3 describes the differences between Hi3521 and Hi3531/Hi3532 APIs by module. For details, see the *Hi3521 Media Processing Software Development Reference*.

Table 1-3 Differences on APIs

| Module | Hi3521 APIs Compared with Hi3531/Hi3532 APIs | Change Description |
|-------------------------|--|--|
| System control | Same | None |
| I/O bind | Same | None |
| Video input unit (VIU) | Slight different | The APIs for setting secondary attributes are added, mixing capture is supported, and the limitations on some parameters are changed. |
| Video output unit (VOU) | Slight different | The LCD HD output API and SD BT656_H/L type (multiplexed with BT.1120) are added. |
| VPP | Slight different | The API for pre-scaling the VPSS group is added. The APIs for setting noise reduction (NR), sharp, and field capture attributes of a channel are added. |
| OSD overlay | Same | None |
| Video encoding (VENC) | Slight different | The VENC APIs of the Hi3521 are the same as those of the Hi3531/Hi3532. However, some functions are not supported. |
| Video decoding (VDEC) | Slight different | The VDEC APIs of the Hi3521 are the same as those of the Hi3531/Hi3532. However, some functions are not supported. |



| Module | Hi3521 APIs Compared with Hi3531/Hi3532 APIs | Change Description |
|------------------------------|--|--------------------|
| Motion detection (MD) | Same | None |
| IVE | Same | None |
| Audio | Same | None |
| Frame buffer | Same | None |
| Two-dimensional engine (TDE) | Same | None |